## AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A semiconductor device comprising:

a semiconductor layer formed on an insulating surface and the semiconductor layer comprising a channel forming region;

a first insulating film formed on the semiconductor layer, [[said]] the first insulating film formed to cover an entire surface of the channel forming region;

a first auxiliary electrode formed over the semiconductor layer with the first insulating film interposed therebetween;

a second insulating film formed on and in contact with the first insulating film and the first auxiliary electrode, the second insulating film formed to cover the entire surface of the channel forming region with the first insulating film interposed therebetween; and

a gate electrode formed over the channel forming region with the first insulating film and second insulating film interposed therebetween,

wherein the first auxiliary electrode is formed outside of the channel forming region.

2. (Original) The semiconductor device according to claim 1, wherein the first insulating film has a thickness of 1 to 100 nm, and the second insulating film has a thickness of 5 to 100 nm.

3. (Previously presented) The semiconductor device according to claim 1, wherein the first insulating film has a thickness of 5 to 50 nm, and the second insulating film has a thickness of 5 to 100 nm.

4. (Original) The semiconductor device according to claim 1, wherein the first auxiliary electrode is partially overlapped with the gate electrode with the second insulating film interposed therebetween.

5. (Original) The semiconductor device according to claim 1, wherein the first auxiliary electrode is formed between the channel forming region and a drain region in the semiconductor layer.

6. (Previously presented) The semiconductor device according to claim 1, wherein a second auxiliary electrode is formed over the semiconductor layer with the first insulating film interposed therebetween, and the second auxiliary electrode is formed between a source region and the channel forming region in the semiconductor layer.

7. (Original) The semiconductor device according to claim 1, wherein an impurity element is included in a portion of the semiconductor layer opposed to the first auxiliary electrode through the first insulating film.

8. (Original) The semiconductor device according to claim 1, wherein a third auxiliary electrode is formed on the second insulating film.

9. (Original) The semiconductor device according to claim 8, wherein the third auxiliary electrode has a curved surface or an inclined surface.

10. (Currently Amended) A semiconductor device comprising ~~including~~:

a semiconductor layer comprising a channel forming region;

a first insulating film formed on the semiconductor layer, [[said]] the first insulating film formed to cover an entire surface of the channel forming region;

a first auxiliary electrode for controlling the carrier density between a source region or a drain region, and the channel forming region in the semiconductor layer;

a second insulating film formed on the first insulating film and the first auxiliary electrode, the second insulating film formed to cover the entire surface of the channel forming region with the first insulating film interposed therebetween; and

a gate electrode formed over the channel forming region with the first insulating film and second insulating film interposed therebetween.

11. (Original) The semiconductor device according to claim 10, wherein the first insulating film has a thickness of 1 to 100 nm, and the second insulating film has a thickness of 5 to 100 nm.

12. (Original) The semiconductor device according to claim 10, wherein the first insulating film has a thickness of 5 to 50 nm, and the second insulating film has a thickness of 5 to 100 nm.

13. (Original) The semiconductor device according to claim 10, wherein the first auxiliary electrode is partially overlapped with the gate electrode with the second insulating film interposed therebetween.

14. (Original) The semiconductor device according to claim 10, wherein the first auxiliary electrode is formed between the channel forming region and the drain region in the semiconductor layer.

15. (Previously presented) The semiconductor device according to claim 10, wherein a second auxiliary electrode is formed over the semiconductor layer with the first insulating film interposed therebetween, and the second auxiliary electrode is formed between the source region and the channel forming region in the semiconductor layer.

16. (Original) The semiconductor device according to claim 10, wherein an impurity element is included in a portion of the semiconductor layer opposed to the first auxiliary electrode through the first insulating film.

17. (Original) The semiconductor device according to claim 10, wherein a third auxiliary electrode is formed on the second insulating film.

18. (Original) The semiconductor device according to claim 17, wherein the third auxiliary electrode has a curved surface or an inclined surface.

19. (Original) A semiconductor device comprising:

a first thin film transistor over a substrate, the first thin film transistor comprising a first semiconductor layer, a first gate insulating film, and a first gate electrode;

a second thin film transistor over the substrate, the second thin film transistor comprising a second semiconductor layer, a second gate insulating film having a first film and a second film, and a second gate electrode; and

a first auxiliary electrode formed between the first film and the second film,

wherein the first auxiliary electrode is formed outside of a channel forming region in the second semiconductor layer, and

wherein the first gate insulating film is thinner than the second gate insulating film.

20. (Original) The semiconductor device according to claim 19, wherein one of the first film and the second film is a same film as the first gate insulating film.

21. (Previously presented) The semiconductor device according to claim 19, wherein the first thin film transistor further comprises:

an insulating film covering the first gate electrode and the first gate insulating film; and

a second auxiliary electrode formed on the insulating film.

22. (Original) The semiconductor device according to claim 21, wherein the second auxiliary electrode has a curved surface or an inclined surface.

23. (Original) The semiconductor device according to claim 22, wherein each of the first auxiliary electrode, the second auxiliary electrode, the first gate electrode, and the second gate electrode are connected to a different wiring.

24. (Previously presented) The semiconductor device according to claim 19, wherein the first gate insulating film has a thickness of 1 to 100 nm thick, and the second gate insulating film has a thickness of 6 to 200 nm.

25. (Previously presented) The semiconductor device according to claim 19, wherein the first gate insulating film has a thickness of 5 to 50 nm thick, and the second gate insulating film has a thickness of 6 to 200 nm.

26. (Original) The semiconductor device according to claim 19, wherein the first auxiliary electrode is formed between a drain region and a channel forming region in the second semiconductor layer.

27. (Currently Amended) The semiconductor device according to claim 19, wherein a third auxiliary electrode is formed between the first film and the second film in the second gate insulating film, [[said]] the third auxiliary electrode is formed between a source region and a channel forming region in the second semiconductor layer.

28. (Original) The semiconductor device according to claim 19, wherein the first auxiliary electrode is partially overlapped with the second gate electrode.

29. (Original) The semiconductor device according to claim 19, wherein each of the first auxiliary electrode, the first gate electrode, and the second gate electrode is connected to a different wiring.

30. (Original) The semiconductor device according to claim 19, wherein an impurity element is included in a portion of the semiconductor layer opposed to the first auxiliary electrode through the second gate insulating film.

31. (Previously presented) A semiconductor device comprising:

a first thin film transistor over a substrate, the first thin film transistor comprising a first semiconductor layer, a first gate insulating film, and a first gate electrode;

a second thin film transistor over the substrate, the second thin film transistor comprising a second semiconductor layer, a second gate insulating film having a first film and a second film, and a second gate electrode;

a first auxiliary electrode for controlling the carrier density between a source region or drain region and a channel forming region in the second semiconductor layer,

wherein the first auxiliary electrode is formed between the first film and the second film, and

wherein the first gate insulating film is thinner than the second gate insulating film.

32. (Original) The semiconductor device according to claim 31, wherein one of the first film and the second film is a same film as the first gate insulating film.

33. (Previously presented) The semiconductor device according to claim 31, wherein the first thin film transistor further comprises:

an insulating film covering the first gate electrode and the first gate insulating film; and

a second auxiliary electrode formed on the insulating film.

34. (Original) The semiconductor device according to claim 33, wherein the second auxiliary electrode has a curved surface or an inclined surface.

35. (Original) The semiconductor device according to claim 34, wherein each of the first auxiliary electrode, the second auxiliary electrode, the first gate electrode, and the second gate electrode are connected to a different wiring.

36. (Previously presented) The semiconductor device according to claim 31, wherein the first gate insulating film has a thickness of 1 to 100 nm thick, and the second gate insulating film has a thickness of 6 to 200 nm.

37. (Previously presented) The semiconductor device according to claim 31, wherein the first gate insulating film has a thickness of 5 to 50 nm thick, and the second gate insulating film has a thickness of 6 to 150 nm.

38. (Original) The semiconductor device according to claim 31, wherein the first auxiliary electrode is formed between a drain region and a channel forming region in the second semiconductor layer.

39. (Currently Amended) The semiconductor device according to claim 31, wherein a third electrode is formed between the first film and the second film in the second gate insulating film, [[a]] the third auxiliary electrode is formed between a source region and a channel forming region in the second semiconductor layer.

40. (Original) The semiconductor device according to claim 31, wherein the first auxiliary electrode is partially overlapped with the second gate electrode,

41. (Original) The semiconductor device according to claim 31, wherein each of the first auxiliary electrode, the first gate electrode, and the second gate electrode is connected to a different wiring.

42. (Original) The semiconductor device according to claim 31, wherein an impurity element is included in a portion of the semiconductor layer opposed to the first auxiliary electrode through the second gate insulating film.

43. (Currently Amended) A semiconductor device comprising:

a semiconductor layer formed on an insulating surface and the semiconductor layer comprising a first region, at least one second region, a source region, and a drain region;

a first insulating film formed on the semiconductor layer, [[said]] the first insulating film formed to cover an entire surface of the first region and an entire surface of the second region;

a first auxiliary electrode formed over the semiconductor layer with the first insulating film interposed therebetween;

a second insulating film formed on and in contact with the first insulating film and the first auxiliary electrode, the second insulating film formed to cover the entire surface of the first region with the first insulating film interposed therebetween; and a gate electrode formed over the second insulating film,

wherein the first region overlaps with the gate electrode, with the first insulating film and the second insulating film interposed therebetween, and does not overlap with the first auxiliary electrode,

wherein the first region is formed between the source region and the drain region, the second region is formed between the first region and at least one of the source and drain regions, and

wherein the first auxiliary electrode is formed over the second region with the first insulating film interposed therebetween.

44. (Original) The semiconductor device according to claim 43, wherein the first insulating film has a thickness of 1 to 100 nm, and the second insulating film has a thickness of 5 to 100 nm.

45. (Original) The semiconductor device according to claim 43, wherein the first insulating film has a thickness of 5 to 50 nm, and the second insulating film has a thickness of 5 to 100 nm.

46. (Original) The semiconductor device according to claim 43, wherein the first auxiliary electrode is partially overlapped with the gate electrode with the second insulating film interposed therebetween.

47. (Original) The semiconductor device according to claim 43, wherein an impurity element is included in the second region.

48. (Original) The semiconductor device according to claim 43, wherein a second auxiliary electrode is formed on the second insulating film.

49. (Original) The semiconductor device according to claim 48, wherein the second auxiliary electrode has a curved surface or an inclined surface.

50. (Original) The semiconductor device according to claim 43, wherein the first auxiliary electrode controls the carrier density between the source region, the drain region, and the first region.

51. (Original) A semiconductor device comprising:

a first semiconductor layer comprising a first region, a first source region, and a first drain region;

a second semiconductor layer comprising a second region, at least one third region, a second source region, and a second drain region;

a first insulating film formed on the first and second semiconductor layers;

a first auxiliary electrode formed over the second semiconductor layer with the first insulating film interposed therebetween;

a first gate electrode formed over the first semiconductor layer with the first insulating film interposed therebetween;

a second insulating film formed on the first insulating film, the first auxiliary electrode, and the first gate electrode; and

a second gate electrode formed over the second region with the first and second insulating films interposed therebetween,

wherein the second region is formed between the second source region and the second drain region, the third region is formed between the second region and at least one of the second source and drain regions, and

wherein the first auxiliary electrode is formed over the third region with the first insulating film interposed therebetween.

52. (Original) The semiconductor device according to claim 51, wherein the first insulating film has a thickness of 1 to 100 nm, and the second insulating film has a thickness of 5 to 100 nm.

53. (Original) The semiconductor device according to claim 51, wherein the first insulating film has a thickness of 5 to 50 nm, and the second insulating film has a thickness of 5 to 100 nm.

54. (Original) The semiconductor device according to claim 51, wherein the first auxiliary electrode is partially overlapped with the second gate electrode with the second insulating film interposed therebetween.

55. (Original) The semiconductor device according to claim 51, wherein an impurity element is included in the third region.

56. (Original) The semiconductor device according to claim 51, wherein a second auxiliary electrode is formed on the second insulating film.

57. (Original) The semiconductor device according to claim 56, wherein the second auxiliary electrode has a curved surface or an inclined surface.

58. (Original) The semiconductor device according to claim 51, wherein the first auxiliary electrode controls the carrier density between the second source region, the second drain region, and the third region.

59-63. (Canceled).

64. (Previously presented) The semiconductor device according to claim 1, wherein a first distance between the gate electrode and the semiconductor layer is longer than a second distance between the first auxiliary electrode and the semiconductor layer.

65. (Previously presented) The semiconductor device according to claim 10, wherein a first distance between the gate electrode and the semiconductor layer is longer than a second distance between the first auxiliary electrode and the semiconductor layer.

66. (Previously presented) The semiconductor device according to claim 19, wherein a first distance between the second gate electrode and the second semiconductor

layer is longer than a second distance between the first auxiliary electrode and the second semiconductor layer.

67. (Previously presented) The semiconductor device according to claim 31, wherein a first distance between the second gate electrode and the second semiconductor layer is longer than a second distance between the first auxiliary electrode and the second semiconductor layer.

68. (Previously presented) The semiconductor device according to claim 43, wherein a first distance between the gate electrode and the semiconductor layer is longer than a second distance between the first auxiliary electrode and the semiconductor layer.

69. (Previously presented) The semiconductor device according to claim 51, wherein a first distance between the second gate electrode and the second semiconductor layer is longer than a second distance between the first auxiliary electrode and the second semiconductor layer.

70. (New) A semiconductor device comprising:

a semiconductor layer formed on an insulating surface and the semiconductor layer comprising a first region, at least one second region, a source region, and a drain region;

a first insulating film formed on the semiconductor layer, the first insulating film formed to cover an entire surface of the first region and an entire surface of the second region;

a first auxiliary electrode formed over the semiconductor layer with the first insulating film interposed therebetween;

a second insulating film formed on and in contact with the first insulating film and the first auxiliary electrode; and

a gate electrode formed over the second insulating film,

wherein the first region overlaps with the gate electrode, with the first insulating film and the second insulating film interposed therebetween, and does not overlap with the first auxiliary electrode, wherein the first region is formed between the source region and the drain region, the second region is formed between the first region and at least one of the source and drain regions,

wherein the first auxiliary electrode is formed over the second region with the first insulating film interposed therebetween, and

wherein the second region functions as a LDD region by applying a voltage to the first auxiliary electrode.

71. (New) The semiconductor device according to claim 70, wherein the first insulating film thickness of 1 to 100 nm, and the second insulating film has a thickness of 5 to 100 nm.

72. (New) The semiconductor device according to claim 70, wherein the first insulating film has a thickness of 5 to 50 nm, and the second insulating film has a thickness of 5 to 100 nm.

73. (New) The semiconductor device according to claim 70, wherein the first auxiliary electrode is partially overlapped with the gate electrode with the second insulating film interposed therebetween.

74. (New) The semiconductor device according to claim 70, wherein an impurity element is included in the second region.

75. (New) The semiconductor device according to claim 70, wherein a second auxiliary electrode is formed on the second insulating film.

76. (New) The semiconductor device according to claim 70, wherein the second auxiliary electrode has a curved surface or an inclined surface.

77. (New) The semiconductor device according to claim 70, wherein the first auxiliary electrode controls the carrier density between the source region, the drain region, and the first region.

78. (New) The semiconductor device according to claim 70, wherein a first distance between the gate electrode and the semiconductor layer is longer than a second distance between the first auxiliary electrode and the semiconductor layer.